

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT08 Quad 2-input AND gate

Product specification  
File under Integrated Circuits, IC06

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Philips



PHILIPS

## Quad 2-input AND gate

## 74HC/HCT08

## FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

## QUICK REFERENCE DATA

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 15 \text{ pF}$ ; $V_{CC} = 5 \text{ V}$	7	11	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

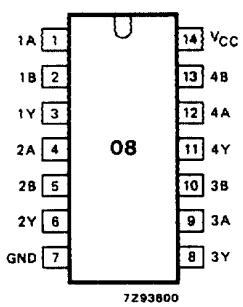


Fig.1 Pin configuration.

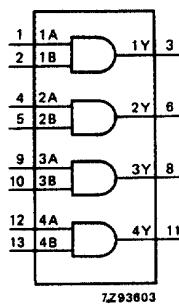


Fig.2 Logic symbol.

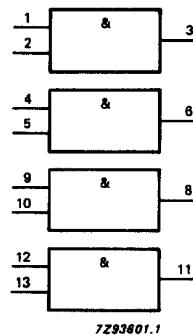


Fig.3 IEC logic symbol.

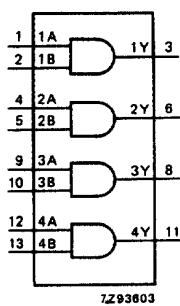


Fig.4 Functional diagram.

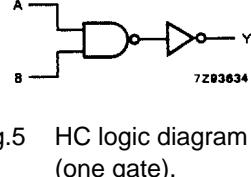


Fig.5 HC logic diagram (one gate).

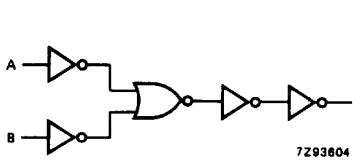


Fig.6 HCT logic diagram (one gate).

## FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

## Note

1. H = HIGH voltage level  
L = LOW voltage level

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>cc</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7	

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

 $I_{CC}$  category: SSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

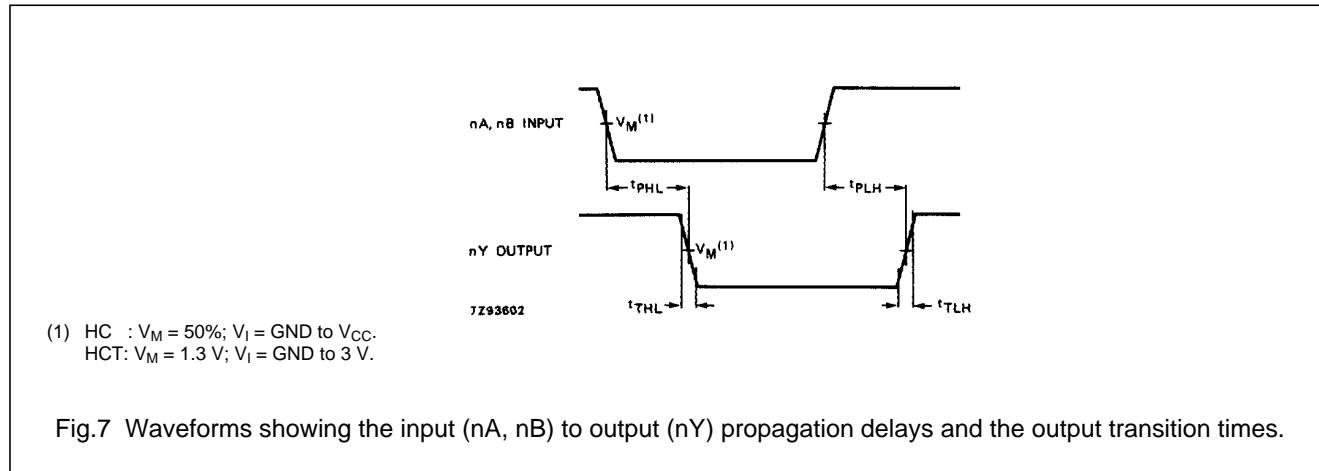
INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS				
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
$t_{PHL}/ t_{PLH}$	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig.7			
$t_{THL}/ t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.7			

## AC WAVEFORMS



## PACKAGE OUTLINES

See "[74HC/HCT/HCU/HCMOS Logic Package Outlines](#)".